# Fundamentals of Analog & Mixed Signal VLSI Design

## Basic Building Blocks

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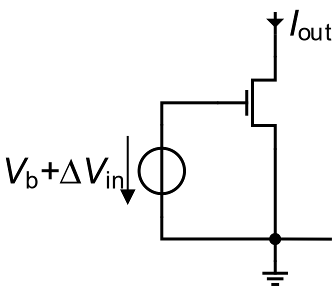
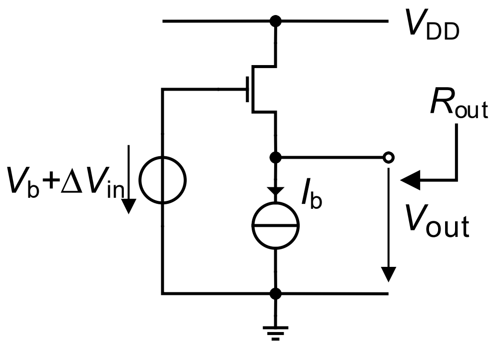
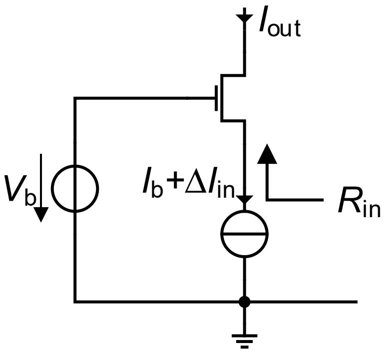
# Outline

- **Introduction**
- Elementary gain cells (common-source stages)
- Source follower (common-drain stages)
- Cascode stage (common-gate stages)
- Current mirrors
- Differential pair
- Current references

# Single-transistor Stages

| Common Source | Common Drain | Common Gate |
| --- | --- | --- |
|  |  |  |
| Transconductance amplifier | Source follower | Cascode |
| $\Delta I_{out} = G_m \cdot \Delta V_{in}$ | $\Delta V_{out} = \Delta V_{in}$ | $\Delta I_{out} = \Delta I_{in}$ |
| | $R_{out} = \dfrac{1}{G_{ms}}$ | $R_{in} = \dfrac{1}{G_{ms}}$ |

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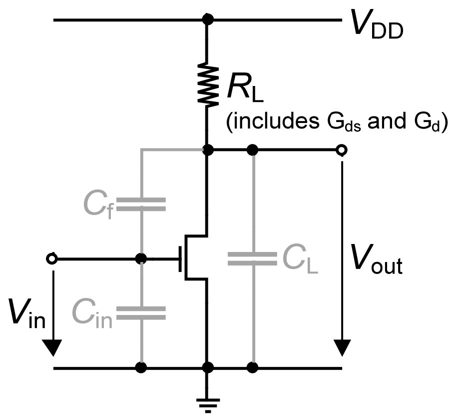
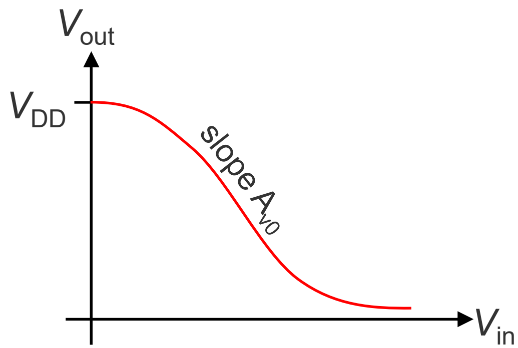
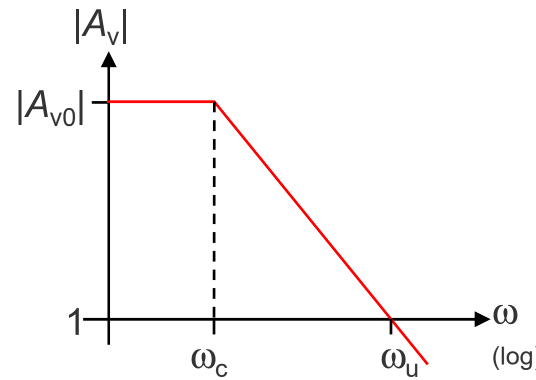
# Elementary Voltage-gain Cells




DC Transfer Characteristic




Small-signal Transfer Function

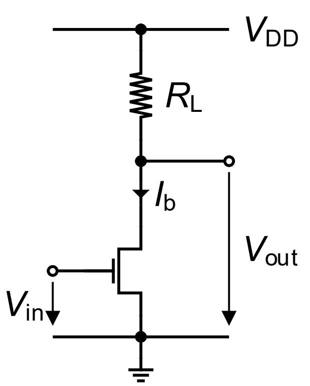


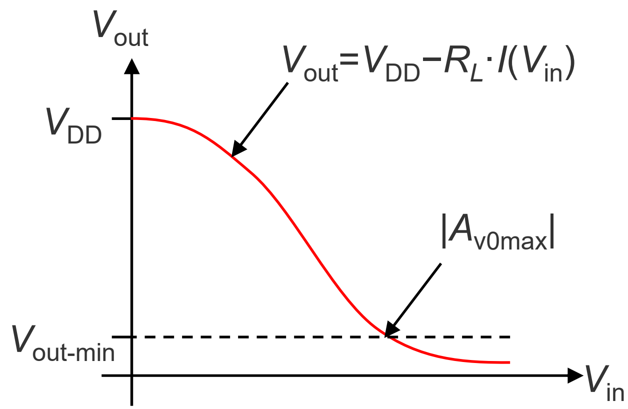

$$A_v = \frac{A_{v0}}{1+\frac{s}{\omega_c}} = \frac{-\omega_u}{s+\omega_c} \cong -\frac{1}{s\tau} \text{ for } \omega \gg \omega_c$$

- where $A_{v0} = -G_m R_L$ is the DC gain, $\omega_c = \frac{1}{R_L(C_f+C_L)}$ the cut-off frequency and $\omega_u = \frac{1}{\tau} = \frac{G_m}{C_f+C_L}$ the unity-gain frequency
- The input admittance $Y_{in}$ is given by

$$Y_{in} = sC_{in} + sC_f(1-A_v) = s\left(C_{in}+C_f\right) + \underbrace{\left(-sC_f A_v\right)}_{\substack{=G_m\frac{C_f}{C_f+C_L} \\ for\ \omega\gg\omega_c}}$$

# Gain Cell with Resistive Load




- The DC gain is given by

$$|A_{v0}| \triangleq \left|\frac{\Delta V_{out}}{\Delta V_{in}}\right| = G_m R_L = \frac{G_m}{I_b} \cdot R_L I_b = \frac{G_m}{I_b} \cdot (V_{DD} - V_{out}) \text{ with } \frac{G_m}{I_b} = \begin{cases} \dfrac{2}{n\, V_{DSsat}} & \text{SI} \\ \dfrac{1}{n\, U_T} & \text{WI} \end{cases}$$

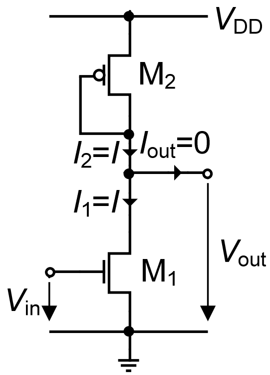
- which is maximum for highest $G_m/I_b$ (WI) and highest $R_L$ and current, hence lowest output voltage that still keeps the transistor in saturation $V_{out,min} = V_{DSsat}$

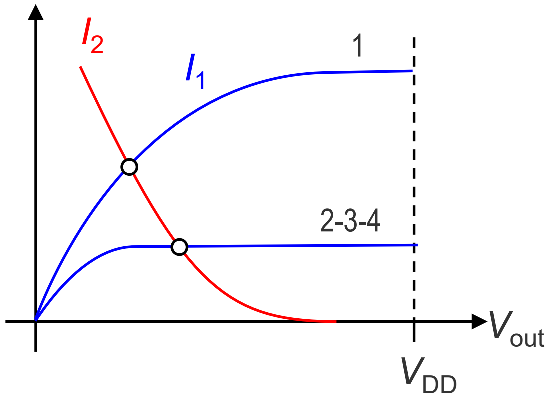
$$|A_{v0}| < \frac{V_{DD}}{n\, U_T}$$

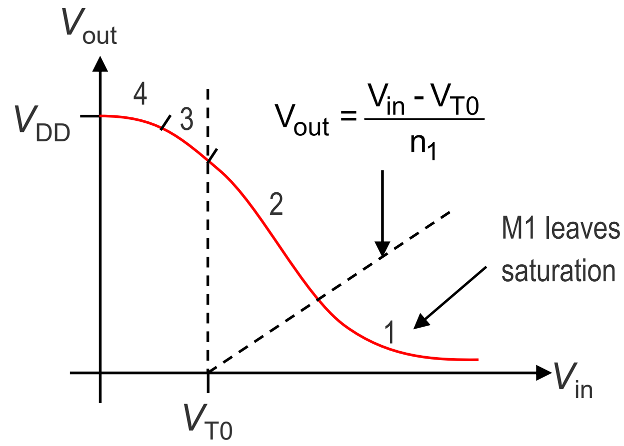
- For $V_{DD} = 1.6\, V$ and $nU_T = 40\, mV$, we have $|A_{v0}| < 40$
- The input-referred noise is dominated by the transistor if $|A_{v0}| \gg 1$
- For thermal noise we have

$$R_{neq} = \frac{\gamma_{neq}}{G_m} \text{ with } \gamma_{neq} = \gamma_n + \frac{1}{G_m R_L} \cong \gamma_n \text{ for } |A_{v0}| = G_m R_L \gg 1$$

# Gain Cell with Diode-connected Load




- Small-signal voltage gain assuming $M_1$ is in saturation

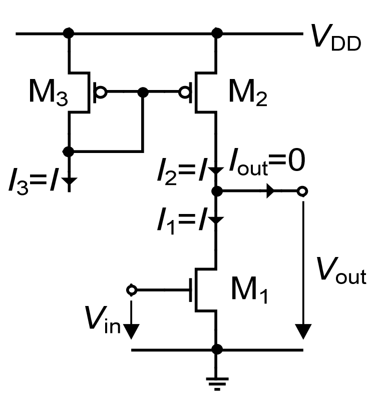
$$|A_{v0}| = \frac{G_{m1}}{G_{m2}} = \begin{cases} \sqrt{\frac{\beta_1 n_2}{\beta_2 n_1}} = \frac{n_2}{n_1} \frac{V_{DSsat2}}{V_{DSsat1}} & \text{M1, M2 in SI (2)} \\ \frac{1}{n_1 U_T} \sqrt{\frac{n_2\, I}{2\beta_2}} = \frac{n_2}{n_1} \frac{V_{DSsat2}}{2U_T} & \text{M1 in WI and M2 in SI (3)} \\ \frac{n_2}{n_1} \cong 1 & \text{M1, M2 in WI (4)} \end{cases}$$

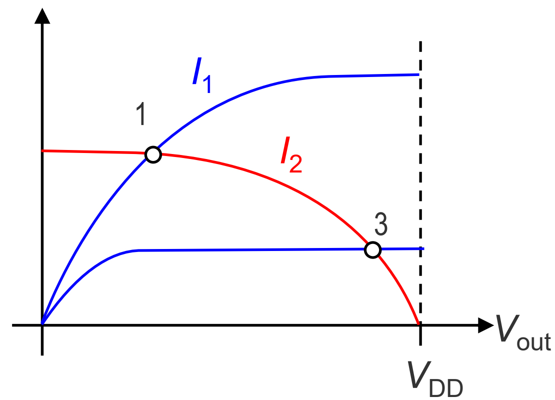
| Region | M1 | M2 |
|---|---|---|
| 1 | SI lin | SI sat |
| 2 | SI sat | SI sat |
| 3 | WI sat | SI sat |
| 4 | WI sat | WI sat |

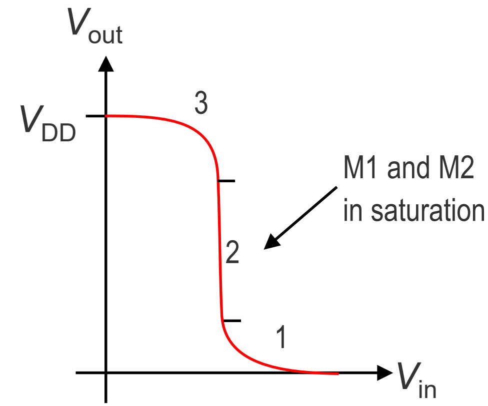
- Maximum for case (3) for which $|A_{v0}| < V_{DD}/(2U_T)$ (30.8 for $V_{DD} = 1.6\ V$)
- Equivalent input-referred noise

$$R_{neq} = R_{n1} + \frac{R_{n2}}{|A_{v0}|^2} \cong R_{n1} \text{ for } |A_{v0}| \gg 1$$

# Gain Cell with Current Source Load




- Small-signal voltage gain assuming $M_1$ and $M_2$ in saturation

$$|A_{v0}| = \frac{G_{m1}}{G_{ds1}+G_{ds2}} = \begin{cases} V_M\sqrt{\frac{2\beta_1}{n_1\, I}} = \frac{2V_M}{n_1 V_{DSsat1}} & \text{M1 in SI} \\ \frac{V_M}{n_1 U_T} & \text{M1 in WI} \end{cases} \quad \text{with } \frac{1}{V_M} = \frac{1}{V_{M1}} + \frac{1}{V_{M2}}$$

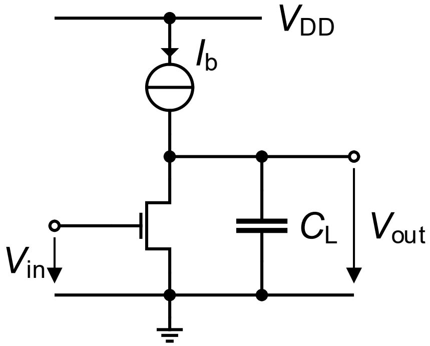
- Equivalent input-referred thermal noise

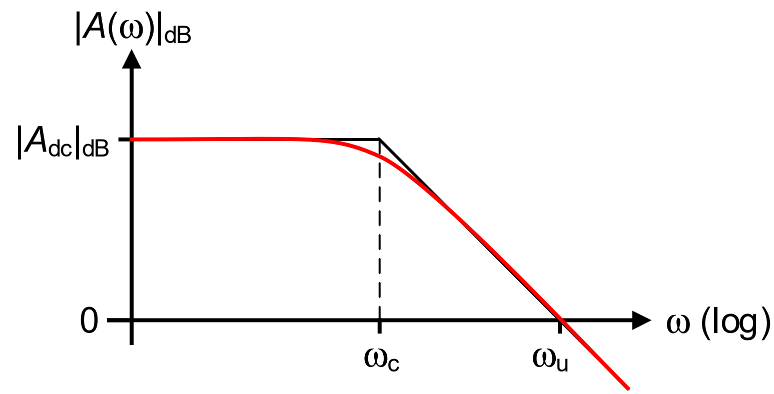
$$R_{neq} = R_{n1} + \left(\frac{G_{m2}}{G_{m1}}\right)^2 (R_{n2} + R_{n3})$$

- Contribution of $M_2$ and $M_3$ minimized with $M_2$ in SI and $M_1$ in WI

$$R_{neq} = R_{n1} + \left(\frac{2n_1 U_T}{V_{DSsat2}}\right)^2 (R_{n2} + R_{n3})$$

# Gain, Bandwidth and Gain-bandwidth Product




- The small-signal **voltage gain** (or transfer function) is given by

$$A_v \triangleq \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{A_{dc}}{1+\frac{s}{\omega_c}} \text{ with } A_{dc} = -\frac{G_m}{G_{ds}} \text{ the DC gain and } \omega_c = \frac{G_{ds}}{C_L} \text{ the bandwidth}$$

- $\omega_u$ is the **unity gain frequency** which for $|A_{dc}| \gg 1$ is equal to

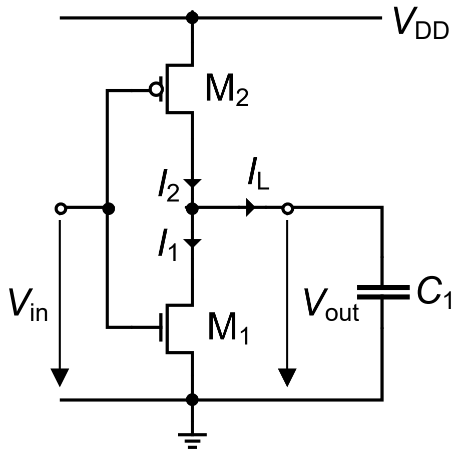
$$\omega_u \cong |A_{dc}| \cdot \omega_c = \frac{G_m}{C_L} \text{ for } |A_{dc}| \gg 1$$

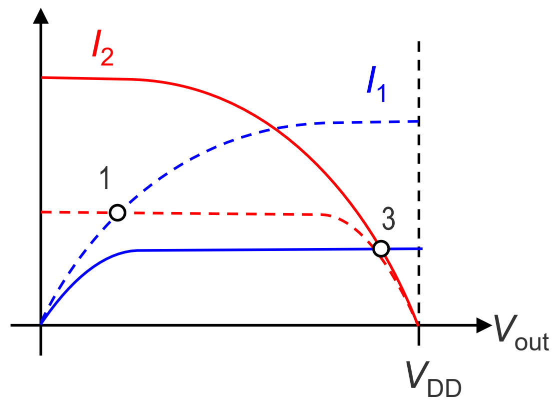
- which corresponds to the **gain-bandwidth product**

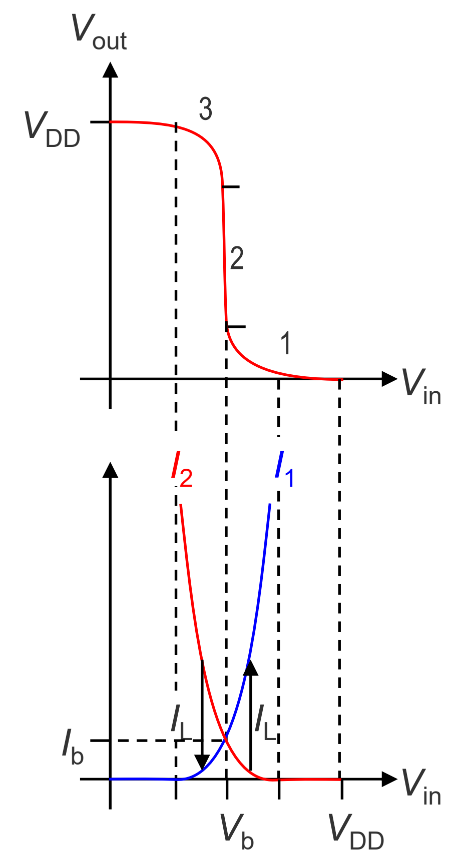
$$GBW = \frac{\omega_u}{2\pi} \cong |A_{dc}| \cdot BW = \frac{G_m}{2\pi C_L} \text{ for } |A_{dc}| \gg 1$$

- It is the **most important feature** of a transconductance amplifier

# CMOS Inverter as a Gain Cell



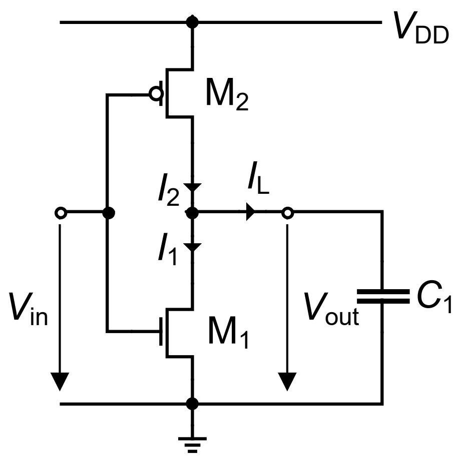

- DC gain for $M_1$ and $M_2$ in saturation

$$|A_{v0}| = \frac{G_{m1} + G_{m2}}{G_{ds1} + G_{ds2}} = \begin{cases} \dfrac{V_M}{nU_T} & \text{M1, M2 in WI} \\[2ex] \dfrac{V_M}{\sqrt{I_b}} \left( \sqrt{\dfrac{2\beta_1}{n_1}} + \sqrt{\dfrac{2\beta_2}{n_2}} \right) & \text{M1, M2 in SI} \end{cases}$$

- where

$$\frac{1}{V_M} = \frac{1}{V_{M1}} + \frac{1}{V_{M2}} \text{ and } \frac{1}{n} = \frac{1}{n_1} + \frac{1}{n_2}$$

# CMOS Inverter as a Gain Cell




- Small-signal DC gain: $A_{v0} = -\frac{G_{m1}+G_{m2}}{G_{ds1}+G_{ds2}}$
- Transconductance: $G_m = G_{m1} + G_{m2}$
- Input-referred noise:

$$R_{neq} = \frac{G_{m1}^2 \cdot R_{n1} + G_{m2}^2 \cdot R_{n2}}{(G_{m1} + G_{m2})^2} \cong \frac{R_{n1}}{2}$$

- Maximum DC gain
- Maximum transconductance at given current $I_b$
- Minimum input-referred white noise at given current $I_b$
- Intrinsically class AB
- Linear transconductor in SI and saturation (for $\beta_1/n_1 = \beta_2/n_2$)
- BUT poor intrinsic PSRR (6 dB)!

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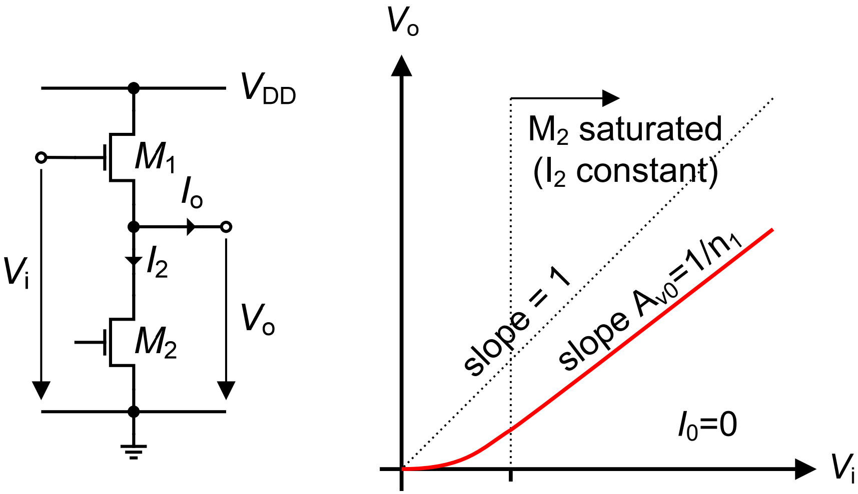
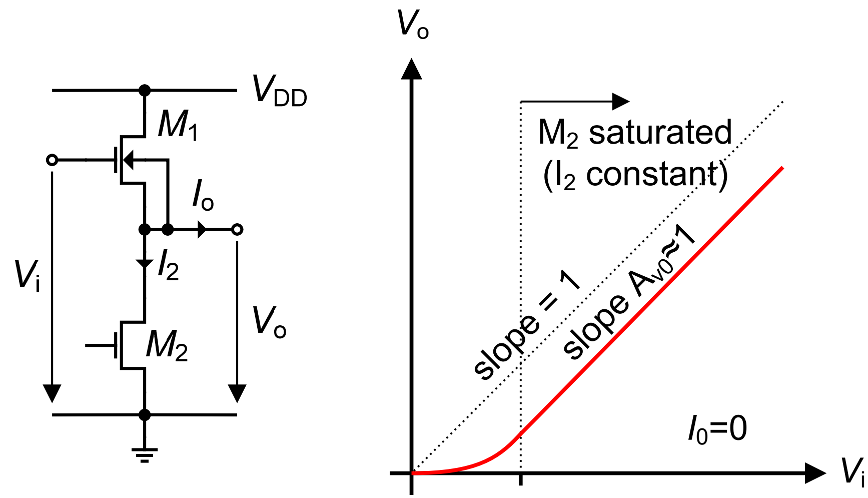
# Source Follower




- $M_1$ in common substrate
- For $M_1$ and $M_2$ saturated and $G_{ds1}, G_{ds} \ll G_{m1} < G_{ms1}$

$$A_{v0} \cong \frac{G_{m1}}{G_{ms1}} = \frac{1}{n_1} < 1$$

- The small-signal voltage gain is smaller than unity

- In case $M_1$ in separate well connected to its source

$$A_{v0} = \frac{1}{1 + G/G_{m1}} \cong 1$$

- with

$$G = G_{ds1} + G_{ds2} + (G_{well} + G_{d2})$$

- where $G_{well}$ and $G_{d2}$ are the differential conductance of the junctions attached to the output node

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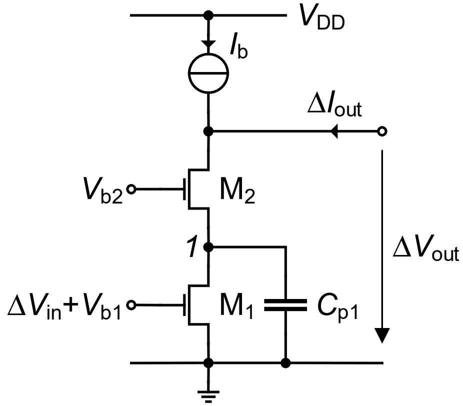
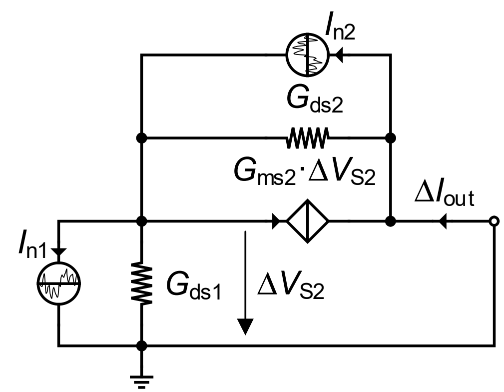
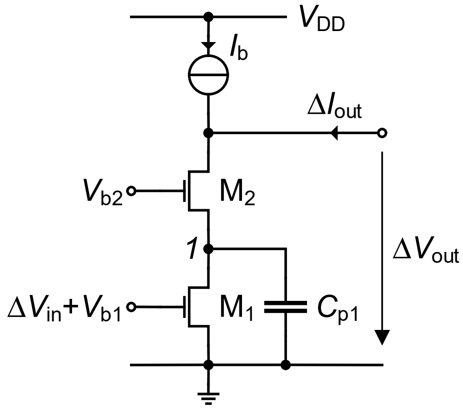
# Cascode Gain Stage – Output Noise



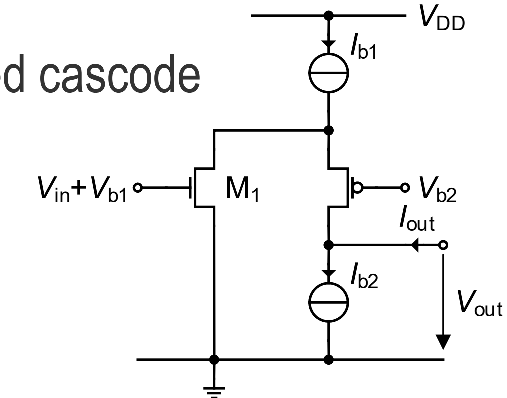




- Output noise current $$I_{nout} \cong I_{n1} + \frac{G_{ds1}}{G_{ms2}} I_{n2}$$
- Output noise conductance $$G_{nout} \cong G_{n1} + \left(\frac{G_{ds1}}{G_{ms2}}\right)^2 G_{n2}$$
- where $$G_{ni} = \gamma_{ni}\, G_{mi} + G_{mi}^2 \, \frac{\rho_n}{W_i\, L_i}$$
- The noise of $M_1$ is fed directly to the output whereas the noise from $M_2$ is divided by the gain $G_{ms2}/G_{ds1}$
- If $G_{ds1} = 0$ the noise current $I_{n2}$ circulates in the cascode transistor M2 and never reaches the output

# Cascode Gain Stage – Principle

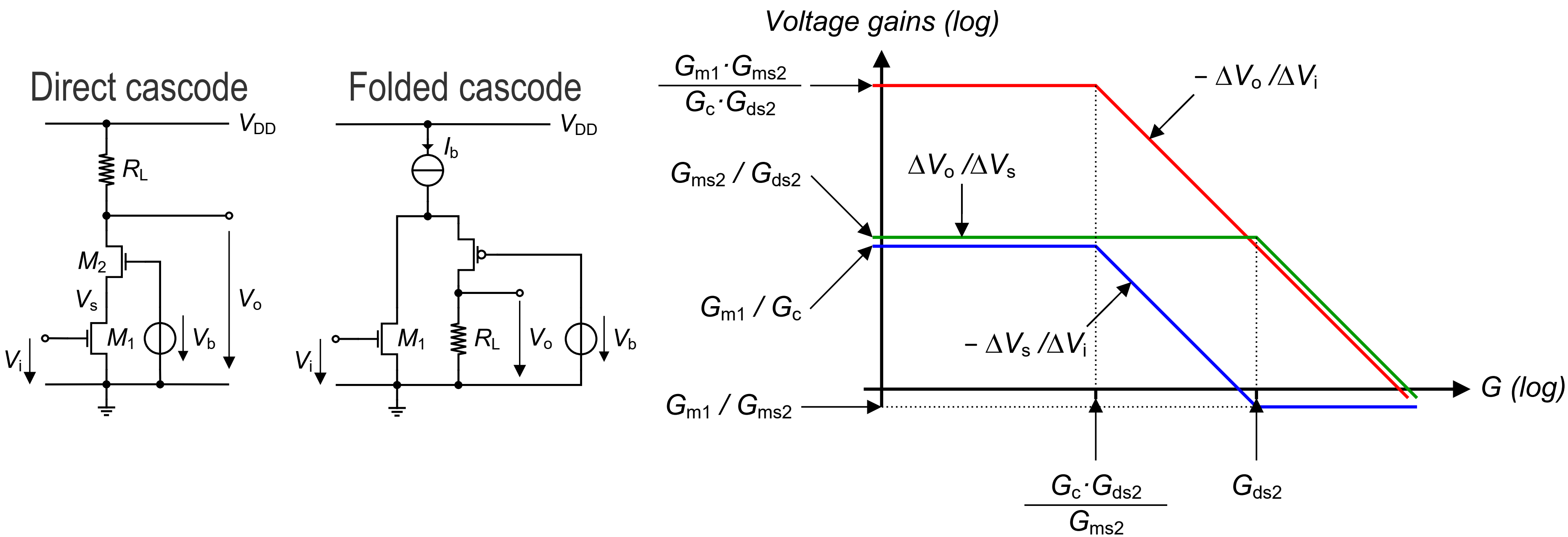



Folded cascode




- Equivalent transconductance $G_{meq} \triangleq \left.\frac{\Delta I_{out}}{\Delta V_{in}}\right|_{\Delta V_{out}=0} \cong G_{m1}$
- Output conductance $G_{out} \cong \frac{G_{ds1}}{G_{ms2}/G_{ds2}}$
- Voltage gain $A_v \triangleq \left.\frac{\Delta V_{out}}{\Delta V_{in}}\right|_{\Delta I_{out}=0} \cong -\frac{G_{m1}}{G_{ds1}} \cdot \frac{G_{ms2}}{G_{ds2}}$
- The voltage gain is equivalent to the cascade of two CS stages i.e. $(G_m/G_{ds})^2$
- The difference is that this gain in the case of the two CS stages requires twice the bias current used in the cascode stage

# Cascode Gain Cell

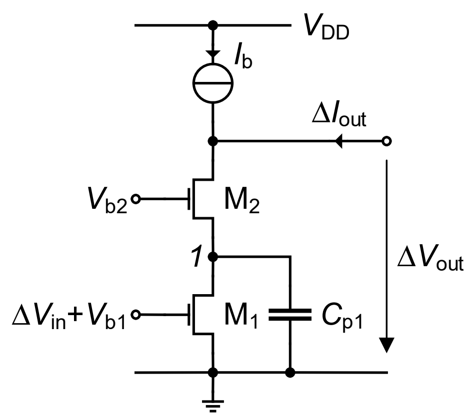


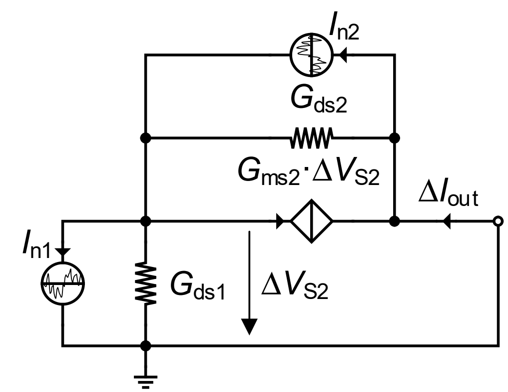

- Small-signal analysis assuming $G_{ms2} \gg G_{ds2}$ yields

$$A_v = \frac{\Delta V_o}{\Delta V_i} = \frac{\Delta V_o}{\Delta V_s} \cdot \frac{\Delta V_s}{\Delta V_i} \text{ with } \frac{\Delta V_o}{\Delta V_s} = \frac{G_{ms2}}{G_{ds2}+G} \text{ and } \frac{\Delta V_s}{\Delta V_i} = -\frac{G_{m1}}{G_c + \frac{G G_{ms2}}{G+G_{ds2}}}$$

- where $G \triangleq G_L + G_{d2}$ and $G_c \triangleq G_{ds1} + G_{d1} + G_{s2}$
- $G_d$, $G_s$ are the small-signal conductances of the source and drain junctions respectively

# Cascode Gain Stage – Input Noise




- Input-referred thermal noise

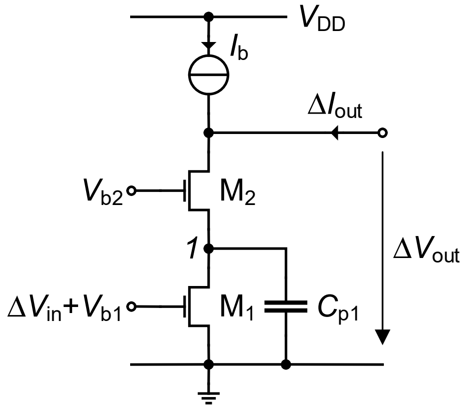
$$R_{n,th} \cong \frac{\gamma_{n1}}{G_{m1}} \cdot (1+\eta_{th}) \cong \frac{\gamma_{n1}}{G_{m1}} \text{ with } \eta_{th} \cong \frac{\gamma_{n2}}{n_2 \gamma_{n1}} \cdot \frac{G_{ds1}^2}{G_{m1} G_{ms2}} \ll 1$$

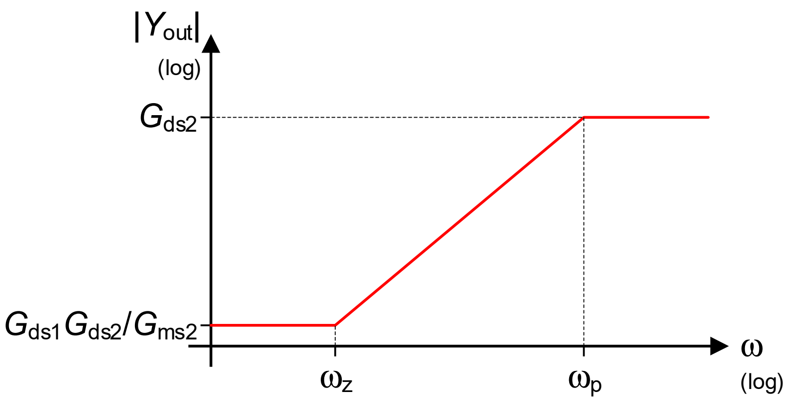
- Input-referred flicker noise

$$R_{n,fl} \cong \frac{\rho_n}{f\, W_1 L_1} \cdot (1+\eta_{fl}) \cong \frac{\rho_n}{f\, W_1 L_1} \text{ with } \eta_{fl} \cong \left(\frac{G_{ds1}}{n_2\, G_{m1}}\right)^2 \frac{W_1 L_1}{W_2 L_2}$$

- The noise of the cascode transistor can be neglected (at low frequency)

# Cascode Gain Stage – Effect of Parasitic Capacitance



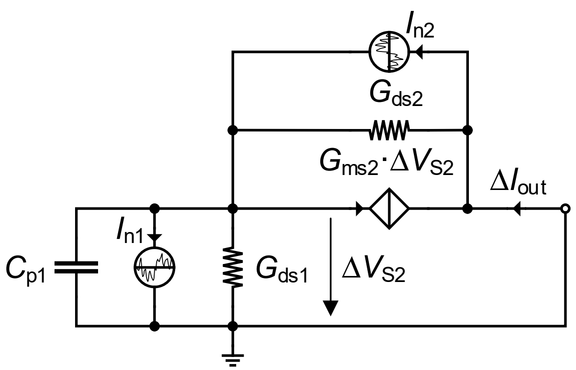



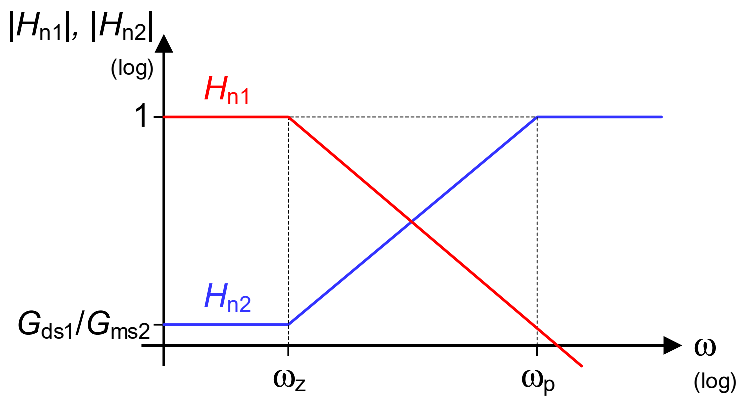

- At high frequency the cascode node 1 is shorted to the ac ground and the increasing the output admittance above $\omega_p$
- The cascode effect is therefore lost at high frequency ($\omega_p < \omega$) due to the parasitic capacitance at node 1 $C_{p1}$

$$Y_{out} = G_{out} \cdot \frac{1 + j\omega/\omega_z}{1 + j\omega/\omega_p} = \begin{cases} G_{out} & \omega \ll \omega_z \\ G_{ds2} & \omega_p \ll \omega \end{cases}$$

- with $G_{out} \cong \frac{G_{ds1}\, G_{ds2}}{G_{ms2}} \ll G_{ds2}$, $\omega_z = \frac{G_{ds1}}{C_{p1}}$ and $\omega_p = \frac{G_{ms2}}{C_{p1}}$

# Cascode Gain Stage – Effect of Parasitic Capacitance



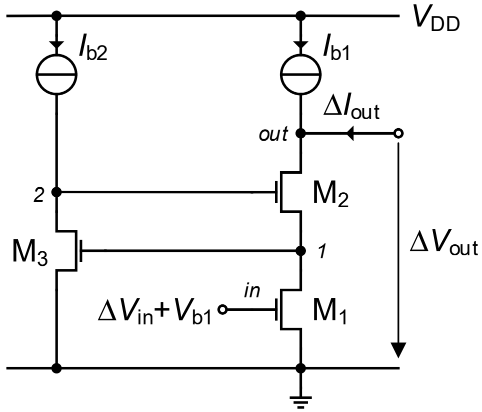



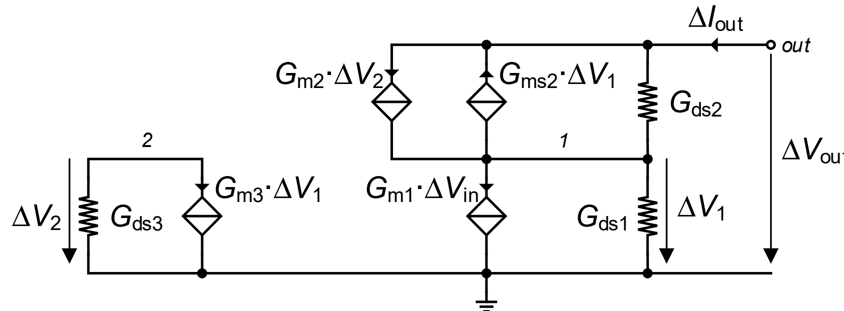

- At high frequency the cascode node 1 is shorted to the ac ground and the noise of the cascode transistor $M_2$ starts to dominate above $\omega_p$
- The output noise is given by

$$G_{nout} = |H_{n1}(\omega)|^2 \cdot G_{n1} + |H_{n2}(\omega)|^2 \cdot G_{n2}$$

- with $H_{n1}(\omega) = \frac{1}{1+j\omega/\omega_p}$ and $H_{n1}(\omega) = \frac{G_{ds1}}{G_{ms2}} \frac{1+j\omega/\omega_z}{1+j\omega/\omega_p}$
- The noise of the cascode transistor $M_2$ can only be neglected below $\omega_z = G_{ds1}/C_{p1}$

# Regulated Cascode – Output Conductance and Gain

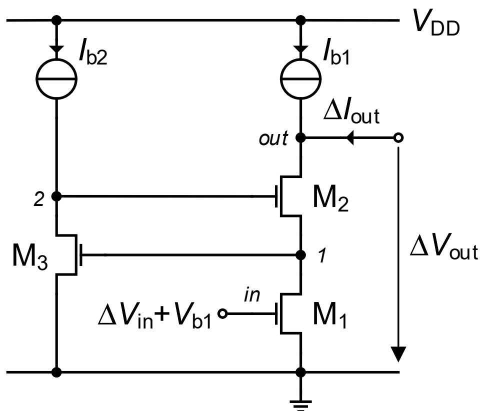


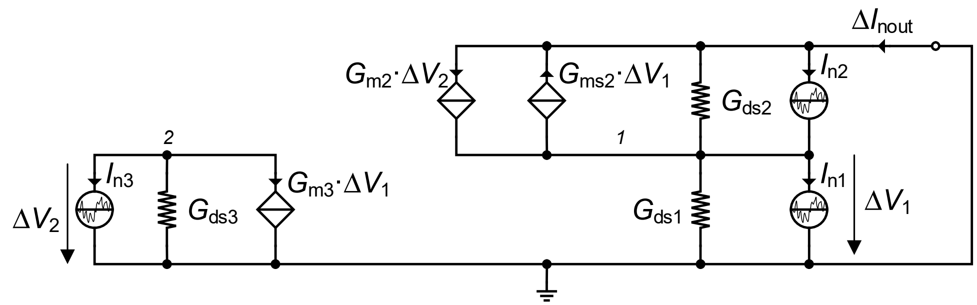




- Equivalent transconductance $G_{meq} \triangleq \left.\frac{\Delta I_{out}}{\Delta V_{in}}\right|_{\Delta V_{out}=0} \cong G_{m1}$
- Output conductance $G_{out} \cong G_{ds1} \frac{G_{ds2}}{G_{m2}} \frac{G_{ds3}}{G_{m3}}$
- Voltage gain $A_v \triangleq \left.\frac{\Delta V_{out}}{\Delta V_{in}}\right|_{\Delta I_{out}=0} \cong -\frac{G_{m1}}{G_{ds1}} \cdot \frac{G_{m2}}{G_{ds2}} \cdot \frac{G_{m2}}{G_{ds2}}$
- which is equivalent to the cascade of three CS gain stages i.e. $(G_m/G_{ds})^3$

E. Sackinger and W. Guggenbuhl, "A high-swing, high-impedance MOS cascode circuit," JSSC, pp. 289–298, 1990.

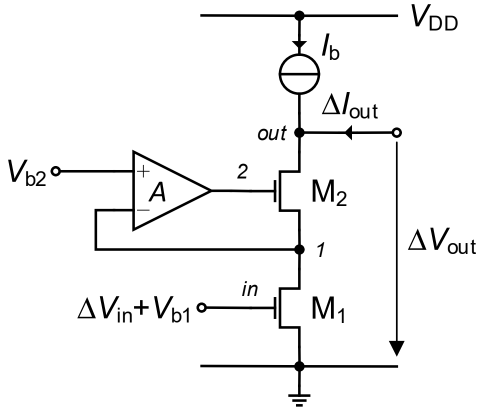
# Regulated Cascode – Noise

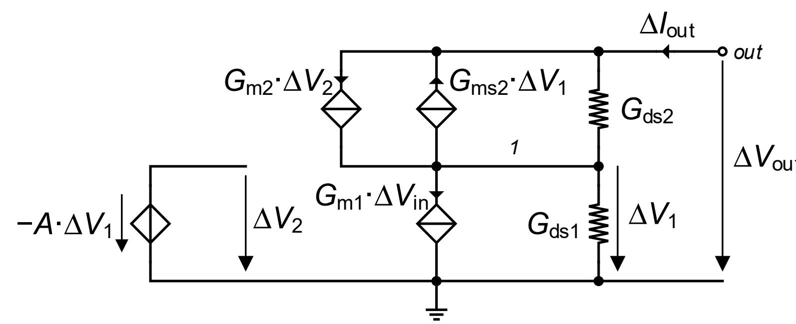



- Input-referred thermal noise $R_{n,th} \cong \frac{\gamma_{n1}}{G_{m1}} \cdot (1+\eta_{th}) \cong \frac{\gamma_{n1}}{G_{m1}}$
- with $\eta_{th} \cong \frac{\gamma_{n2}}{\gamma_{n1}} \cdot \frac{G_{ds1}^2 G_{ds3}^2}{G_{m1} G_{m2} G_{m3}^2} + \frac{\gamma_{n3}}{\gamma_{n1}} \cdot \frac{G_{ds1}^2}{G_{m1} G_{m3}} \ll 1$
- Input-referred flicker noise $R_{n,fl} \cong \frac{\rho_n}{f\, W_1 L_1} \cdot (1+\eta_{fl}) \cong \frac{\rho_n}{f\, W_1 L_1}$
- with $\eta_{fl} \cong \left(\frac{G_{ds1}}{G_{m1}} \frac{G_{ds3}}{G_{m3}}\right)^2 \frac{W_1 L_1}{W_2 L_2} + \left(\frac{G_{ds1}}{G_{m1}}\right)^2 \frac{W_1 L_1}{W_3 L_3}$
- can be made $\eta_{fl} \ll 1$ assuming $M_1$, $M_2$ and $M_3$ have about the gate area
- The noise of the cascode and CS transistors can be neglected (at low frequency)

# Gain Boosting – Principle

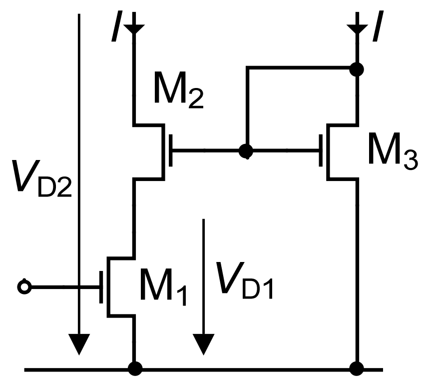



- The regulated cascode is a particular case of the gain boosting technique
- Equivalent transconductance $G_{meq} \triangleq \left.\frac{\Delta I_{out}}{\Delta V_{in}}\right|_{\Delta V_{out}=0} \cong G_{m1}$ for $A \gg n_2$
- Output conductance $G_{out} \cong G_{ds1} \frac{G_{ds2}}{G_{m2}} \frac{1}{A}$ for $A \gg n_2$
- Voltage gain $A_v \triangleq \left.\frac{\Delta V_{out}}{\Delta V_{in}}\right|_{\Delta I_{out}=0} \cong -\frac{G_{m1}}{G_{ds1}} \cdot \frac{G_{m2}}{G_{ds2}} \cdot A$ for $A \gg n_2$
- which correspond to the regulated cascode if $A = G_{m3}/G_{ds3}$, but $G_{out}$ can be made much smaller and $A_v$ much larger for a larger amplifier gain $A$

📖 K. Bult and G. J. G. M. Geelen, "A fast-settling CMOS op amp for SC circuits with 90-dB DC gain," JSSC, vol. 25, no. 6, pp. 1379–1384, 1990.
📖 K. Bult and G. J. G. M. Geelen, "The CMOS gain-boosting technique," Analog Integrated Circuits and Signal Processing, vol. 1, no. 2, pp. 119–135, 1991

# Low-voltage Cascode Bias – Strong Inversion




- Assuming all transistors are biased in strong inversion and in saturation

$$I_{Dk} = \frac{n_k \beta_k}{2}(V_{Pk} - V_{Sk})^2 \text{ for } k = 1,2,3$$

- Choosing $\beta_3$ such that $V_{D1} = V_{P1}$ and equating $I_{D1}$, $I_{D2}$ and $I_{D3}$ results in

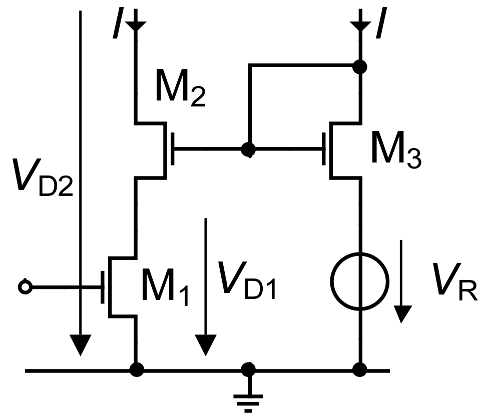
$$\beta_3 = \left(\sqrt{\frac{n_3}{n_1 \beta_1}} + \sqrt{\frac{1}{\beta_2}}\right)^{-2} \cong \left(\sqrt{\frac{1}{\beta_1}} + \sqrt{\frac{1}{\beta_2}}\right)^{-2} \text{ and } V_{P2} = V_{P3} = \frac{V_{P1}}{1 - \sqrt{\beta_3/\beta_2}}$$

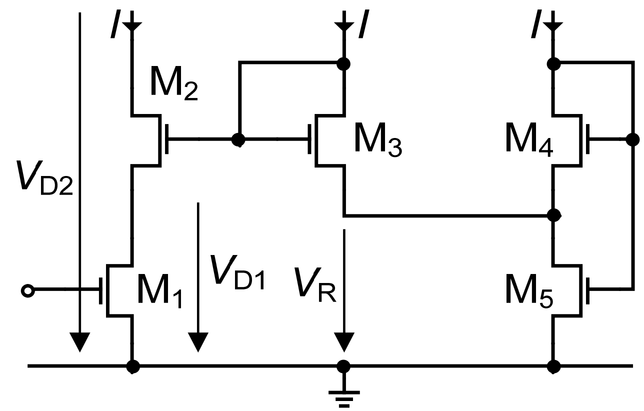
- With the following particular cases

$$\beta_3 \cong \frac{\beta_1}{4} \text{ and } V_{P2} = 2V_{P1} \text{ for } \beta_2 = \beta_1$$

$$\beta_3 \cong \beta_1 \text{ and } V_{P2} \cong V_{P1} \text{ for } \beta_2 \gg \beta_1$$

# Low-voltage Cascode Bias – Weak Inversion




- Assuming all transistors are biased in weak inversion and in saturation
- Voltage source $V_R$ required to have $V_{D1} \approx 4\ to\ 6U_T$ can be realized as shown on the right with

$$V_R = U_T \cdot \ln\left(1 + 2\frac{\beta_4}{\beta_5}\right)$$

- Requires very large $\beta_4/\beta_5$

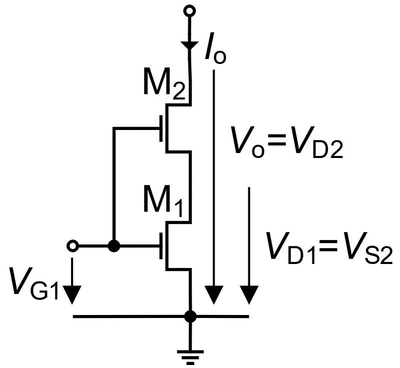
- Can use additional degree of freedom to set $V_{D1} < V_R$ by choosing $\beta_2 > \beta_3$ resulting in

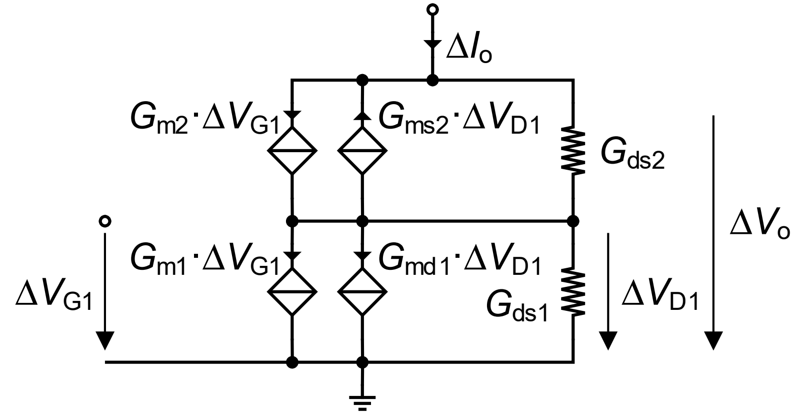
$$V_R = U_T \cdot \ln\left[\frac{\beta_2}{\beta_3}\left(1 + 2\frac{\beta_4}{\beta_5}\right)\right]$$

- Example

$\frac{\beta_2}{\beta_3} = \frac{\beta_4}{\beta_5} = 8$ results in $V_{D1} \cong 5U_T$

# Pseudo-cascode or “Poor Man’s Cascode” (1/2)



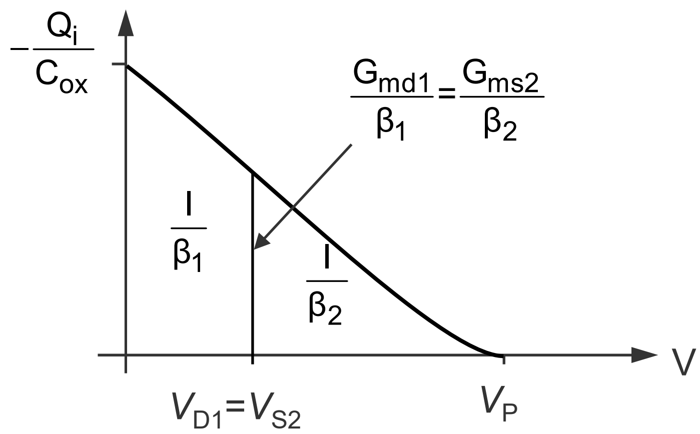




- $M_1$ and $M_2$ have the same gate voltage and thus $V_{D1} < V_{D1sat}$ which means that $M_1$ is biased in the linear region ($G_{md1} > 0$)
- Assuming $M_2$ in saturation and $G_{ms2} \gg G_{ds1}, G_{ds2}$, the output conductance is given

$$G_{out} = \frac{\Delta I_o}{\Delta V_o} = G_{ds2} \cdot \frac{G_{ds1} + G_{md1}}{G_{ms2} + G_{md1} + G_{ds1} + G_{ds2}} \cong G_{ds2} \cdot \frac{G_{ds1} + G_{md1}}{G_{ms2} + G_{md1}}$$

- Since M1 and M2 share the same gate voltage, there is a relation between $G_{md1}$ and $G_{ms2}$ (see next slide)

# Pseudo-cascade or "Poor Man's Cascode" (2/2)




where $G_{md1}$ is the drain transconductance of $M_1$

- Since $M_1$ and $M_2$ share the same gate voltage, we have

$$\frac{G_{md1}}{\beta_1} = \frac{G_{ms2}}{\beta_2} \text{ or } G_{md1} = \frac{\beta_1}{\beta_2} \cdot G_{ms2}$$

- The output conductance then writes

$$G_{out} \cong G_{ds2} \cdot \frac{G_{ds1} + G_{ms2}\,\beta_1/\beta_2}{G_{ms2}(1+\beta_1/\beta_2)}$$

- $G_{out}$ can be reduced by making $M_2$ much wider than $M_1$ and decreasing $\beta_1$ making $M_1$ longer than $M_2$ which allows to assume that $\beta_2 \gg \beta_1$ resulting in

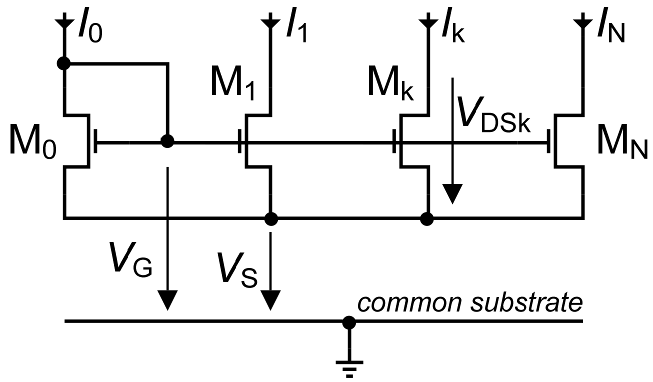
$$G_{out} \cong G_{ds2} \cdot \left(\frac{G_{ds1}}{G_{ms2}} + \frac{\beta_1}{\beta_2}\right)$$

- Note that the first term actually corresponds to the normal cascode

# Outline

- Introduction
- Elementary gain cells (common-source stages)
- Source follower (common-drain stages)
- Cascode stage (common-gate stages)
- **Current mirrors**
- Differential pair
- Current references

# Current Mirrors Principle

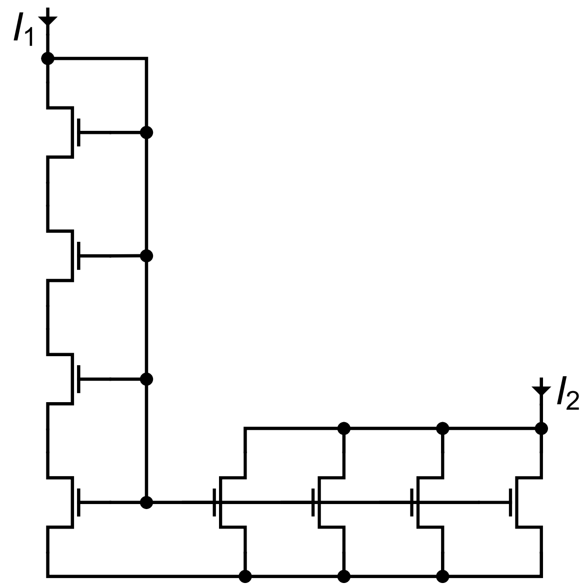



- Assuming that the output conductance can be neglected and all transistors are in saturation, the various output currents are given by

$$\frac{I_k}{I_0} = \frac{I_{speck}}{I_{spec0}} = \frac{\beta_k}{\beta_0} = \begin{cases} 1 & if\ M_k \equiv M_0 \\ \frac{m}{n} & \text{if } m \text{ and } n \text{ transistors in } \| \\ \frac{W_k}{W_0} & \text{any value (but less precision)} \end{cases} \quad \text{for } k = 1 \cdots N$$

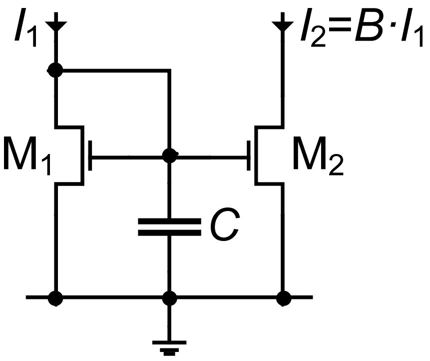
- Keep $L_k / L_0 = 1$ except for $L \gg L_{min}$

# Large Current Ratios




- For implementing large ratios use a combination of series/parallel transistors all in the same substrate (well)
- Example for $I_2/I_1 = 16$
- Less precise than parallel-only transistors (due to channel-length modulation)

# Design Criteria – Precision and Bandwidth




For long-channel:

$$V_{DSsat} \cong \begin{cases} V_P - V_S & \text{SI} \\ 4U_T & \text{WI} \end{cases}$$

- The precision on the currents is limited by the transistor matching

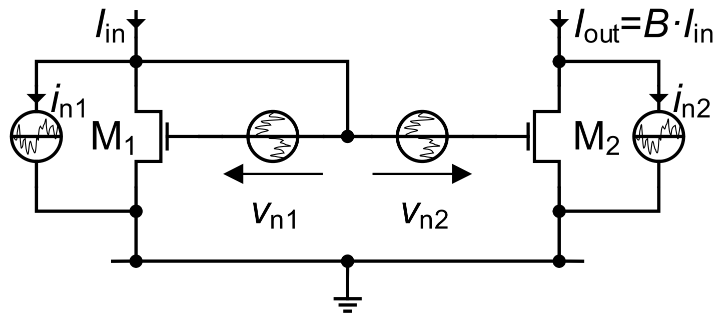
$$\sigma_{\frac{\Delta I_D}{I_D}} = \sqrt{\sigma^2_{\frac{\Delta\beta}{\beta}} + \left(\frac{G_m}{I_D}\right)^2 \sigma^2_{\Delta V_{T0}}} = \frac{1}{\sqrt{WL}} \sqrt{A^2_\beta + \left(\frac{G_m}{I_D}\right)^2 A^2_{\Delta V_{T0}}} \text{ with } \frac{G_m}{I_D} = \begin{cases} \frac{2}{n\,V_{DSsat}} & \text{SI} \\ \frac{1}{n\,U_T} & \text{WI} \end{cases}$$

- The speed is limited by the parasitic capacitance $C$ at the gate node
- The small-signal current gain transfer function is given by

$$\frac{\Delta I_2}{\Delta I_1} = \frac{B}{1+\frac{s}{\omega_c}} \text{ with } \omega_c = \frac{G_{m1}}{C}$$

- where $G_{m1} \propto W \cdot V_{DSsat}$ and $C \propto W$ and hence $\omega_c \propto V_{DSsat}$
- **Matching** and **speed** are therefore **maximized** in strong inversion by **maximizing $V_{DSsat}$**

# Design Criteria – Noise




- Below the cut-off frequency $\omega_c$, the output current noise PSD is given by

$$S_{I_{out}} = B^2\left(S_{I_{in}} + S_{i_{n1}}\right) + G_{m2}^2\left(S_{v_{n1}} + S_{v_{n2}}\right) + S_{i_{n2}}$$

- where $S_{i_{nm}} = 4kT\,\gamma_{nm}\,G_{mm}$ and $S_{v_{nm}} = 4kT\,\dfrac{\rho}{W_m L_m f}$ for $m = 1{,}2$
- In SI, we have $G_{m1} = \dfrac{2I_{in}}{n\,V_{DSsat}}$, $G_{m2} = \dfrac{2BI_{in}}{n\,V_{DSsat}}$ and $\gamma_{n1} = \gamma_{n2} = n\,\dfrac{2}{3}$ and hence $S_{i_{n1}} = kT\,\dfrac{16}{3}\,\dfrac{I_{in}}{V_{DSsat}}$ and $S_{i_{n2}} = kT\,\dfrac{16}{3}\,\dfrac{BI_{in}}{V_{DSsat}}$
- The output noise is then

$$S_{I_{out}} = B^2 S_{I_{in}} + (1+B)kT\,\frac{16}{3}\,\frac{BI_{in}}{V_{DSsat}} + \left(\frac{2BI_{in}}{n\,V_{DSsat}}\right)^2 4kT\,\frac{\rho}{f}\left(\frac{1}{W_1L_1} + \frac{1}{W_2L_2}\right)$$

- **The output current noise** is therefore **minimized** by **maximizing $V_{DSsat}$** or equivalently the inversion factor $IC$ since $V_{DSsat} = 2U_T\cdot\sqrt{IC}$

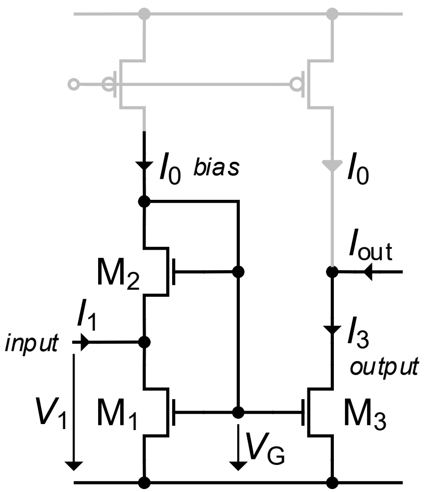
# Current Mirrors Design Procedure

- Select maximum $IC$ or $V_{DSsat}$ compatible with requirements on
  - White noise PSD (avoid $B > 1$ for minimum noise)
  - Speed
  - Relative contribution of $\Delta V_T$ to precision
- Knowing the current $I$, calculate the $W/L$ ratio from

$$\frac{W}{L} = \frac{I}{I_{spec\square} \cdot IC} = \frac{I}{I_{spec\square} \cdot \left(\frac{V_{DSsat}}{2U_T}\right)^2} = \frac{2I}{n\mu C_{ox} V_{DSsat}^2}$$

- Use the second degree of freedom by selecting one of the following
  - $L = L_{min}$ for maximum speed
  - $L$ large enough for large modulation voltage $V_M$ (small output conductance)
  - $WL$ large enough for ensuring required precision and/or limiting 1/f noise
  - $L$ or $W$ minimum for minimum area
- Some specs may not be compatible if $I$ and $V_{DSsat}$ (or $IC$) are imposed

# Low-voltage Current Mirror




- Same local substrate
- M2 and M3 in saturation ($V_{DS} > V_{DSsat}$)
- M1 in linear region ($V_1 < V_{DSsat} < V_G$)

- Assuming $I_1 + I_0 > 0$ (eventually $I_1 \gg I_0$) it can easily be shown that

$$I_3 = \frac{\beta_3(\beta_1 + \beta_2)}{\beta_1 \beta_2} I_0 + \frac{\beta_3}{\beta_1} I_1$$

- In case all transistors are made identical $\beta_1 = \beta_2 = \beta_3$ and

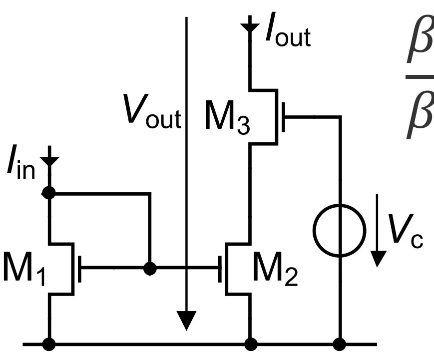
$$I_3 = 2I_0 + I_1$$

- If transistor M2 is made much larger than the other $\beta_2 \gg \beta_1 = \beta_3$ and

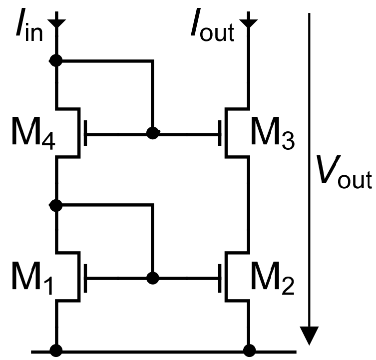
$$I_3 = I_0 + I_1$$

- $I_0$ can be subtracted from $I_3$ to get $I_{out} = I_1$

# Cascode Current Mirror




$$\frac{\beta_4}{\beta_1} = \frac{\beta_3}{\beta_2}$$




By symmetry, $V_{D2} = V_{G2}$ and hence

$$V_{D2} = V_{G2} \gg V_{DSsat2} = V_{P2} \cong \frac{V_{G2} - V_{T0}}{n}$$

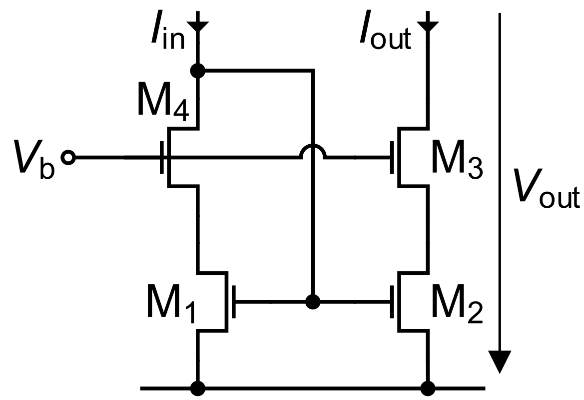
Loss of about $V_{T0}$ voltage across $V_{DS}$ voltage of $M_2$

- Reduce output conductance of current mirror due to channel length modulation ($G_{ds}$) and junction small-signal conductance at the drain ($G_d$)
- Assuming $V_c$ is large enough for biasing $M_2$ in saturation and assuming that all other transistors are biased in saturation, the output conductance is given by

$$G_{out} = \frac{dI_{out}}{dV_{out}} = G_{d3} + (G_{ds2} + G_{d2} + G_{s3}) \cdot \frac{G_{ds3}}{G_{ms3}} \cong G_{d3} + \frac{G_{ds2}}{G_{ms3}/G_{ds3}}$$

- Multiple cascode can be used by stacking additional transistors, but output conductance is ultimately limited by $G_{d3}$
- The bias voltage $V_c$ can be generated as shown on the right schematic but not appropriate for low-voltage

# Low-voltage Cascode Current Mirror

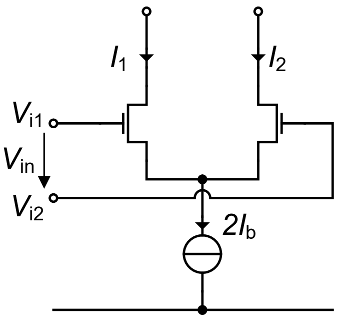



- The above circuit saves some voltage but requires an additional current branch to generate the bias voltage $V_b$
- The bias circuits of the cascode gain stages can be used to generate the bias voltage $V_b$ and bias $M_1$ and $M_2$ at the edge of saturation for maximum output voltage swing

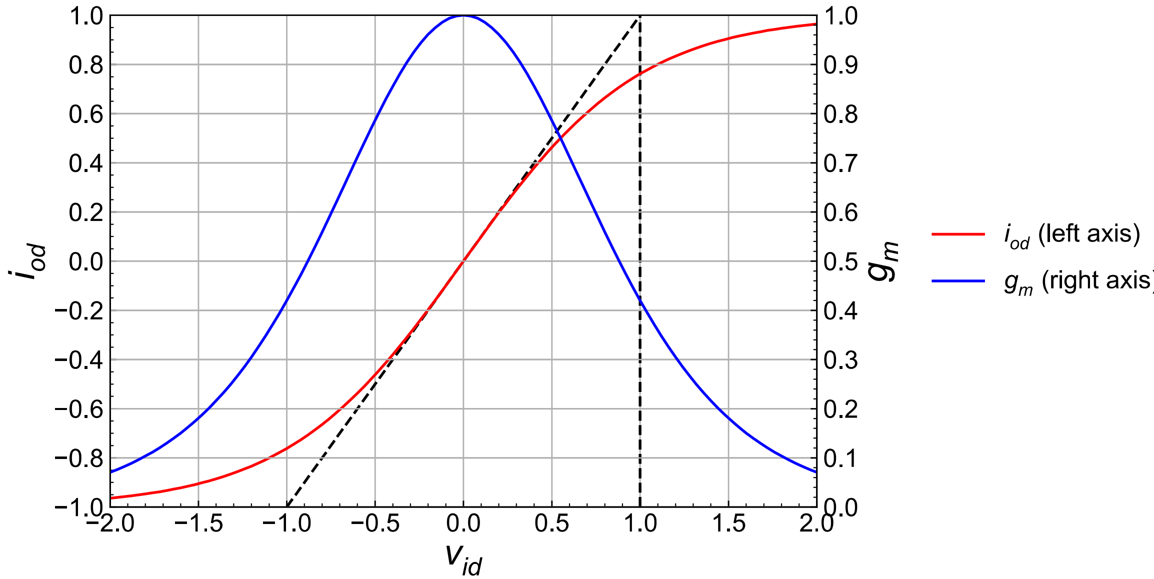
# Outline

- Introduction
- Elementary gain cells (common-source stages)
- Source follower (common-drain stages)
- Cascode stage (common-gate stages)
- Current mirrors
- **Differential pair**
- Current references

# Differential Pair – Weak Inversion




$$I_{od} \triangleq I_1 - I_2$$
$$2I_b = I_1 + I_2$$
$$V_{id} \triangleq V_{i1} - V_{i2}$$
$$V_{ic} \triangleq \frac{V_{i1} + V_{i2}}{2}$$




- In **weak inversion**, the normalized differential output current is given by

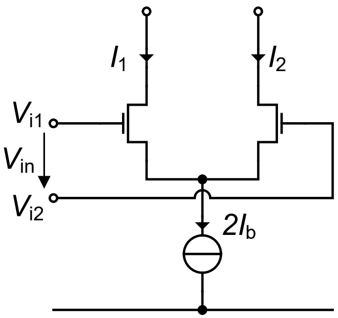
$$i_{od} \triangleq \frac{I_{od}}{2I_b} = \tanh(v_{id}) \text{ with } v_{id} \triangleq \frac{V_{id}}{2nU_T}$$

- and the normalized transconductance by

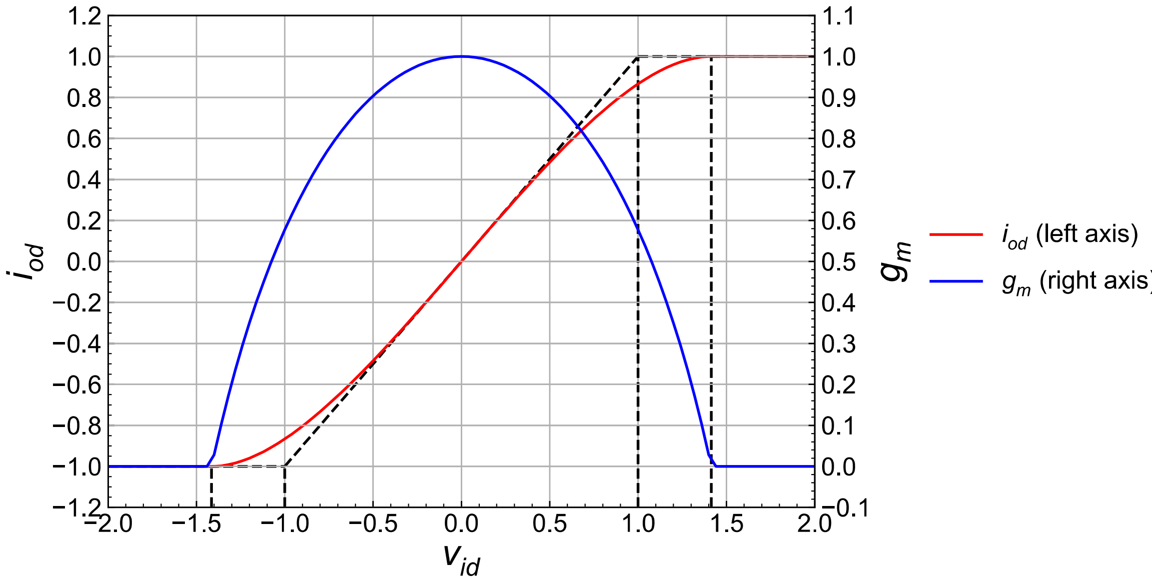
$$g_m \triangleq \frac{G_m}{G_{m0}} = 1 - \tanh^2(v_{id}) \text{ with } G_{m0} \triangleq G_m(0) = \frac{I_b}{nU_T}$$

- Although it offers the **highest current efficiency** $G_{m0}/(2I_b)$, it has the **smallest linear range** ($\cong 4nU_T \cong 155\ mV$)

# Differential Pair – Strong Inversion




$$I_{od} \triangleq I_1 - I_2$$
$$2I_b = I_1 + I_2$$
$$V_{id} \triangleq V_{i1} - V_{i2}$$
$$V_{ic} \triangleq \frac{V_{i1} + V_{i2}}{2}$$




- In **strong inversion**, the normalized differential output current is given by

$$i_{od} \triangleq \frac{I_{od}}{2I_b} = v_{id} \cdot \sqrt{1 - \left(\frac{v_{id}}{2}\right)^2} \text{ for } |v_{id}| \leq \sqrt{2} \text{ with } v_{id} \triangleq \frac{V_{id}}{n\, V_{DSsat}} = \frac{V_{id}}{n(V_p - V_S)} = \frac{V_{id}}{V_G - V_{T0} - nV_S}$$

- and the normalized transconductance by

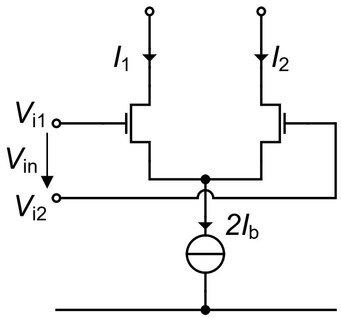
$$g_m \triangleq \frac{G_m}{G_{m0}} = \frac{2 - v_{id}^2}{\sqrt{4 - v_{id}^2}} \text{ with } G_{m0} \triangleq G_m(0) = \sqrt{\frac{2\beta I_b}{n}} = \frac{2I_b}{n\, V_{DSsat}} = \frac{2I_b}{n(V_p - V_S)} = \frac{2I_b}{V_G - V_{T0} - nV_S}$$

- The linear range ($\cong V_G - V_{T0} - nV_S$) can be extended by increasing the overdrive voltage $V_G - V_{T0}$ at the cost of a lower current efficiency

# Differential Pair – In All Modes of Operation

- An expression of the differential input voltage versus the differential output current that is valid in all modes of operation can be found from
  $$\frac{V_{Gk}-V_{T0}-nV_S}{nU_T} = \ln q_{sk} + 2q_{sk} \text{ and } q_{sk} = \tfrac{1}{2}\left(\sqrt{4i_{dk}+1}-1\right) \text{ for } k = 1,2$$
- Normalizing the voltages to $2nU_T$ we get
  $$v_{ik} - v_{t0} - v_s = q_{sk} + \tfrac{1}{2}\ln q_{sk} \text{ for } k = 1,2$$
- The differential voltage is obtained by subtracting the above equations resulting in
  $$v_{id} \triangleq v_{i1} - v_{i2} = q_{s1} - q_{s2} + \tfrac{1}{2}\ln\frac{q_{s1}}{q_{s2}}$$
- Defining the quiescent inversion coefficient $IC_q$ of each transistor as
  $$IC_q \triangleq i_{d1}\Big|_{v_{id}=0} = i_{d2}\Big|_{v_{id}=0} = \frac{I_b}{I_{spec}}$$
- We can then write
  $$q_{s1} = \tfrac{1}{2}\left(\sqrt{4IC_q(1+i_{od})+1}-1\right) \text{ and } q_{s2} = \tfrac{1}{2}\left(\sqrt{4IC_q(1-i_{od})+1}-1\right)$$
- where $i_{od} \triangleq I_{od}/(2I_b) = (I_1 - I_2)/(2I_b)$

# Differential Pair – In All Modes of Operation

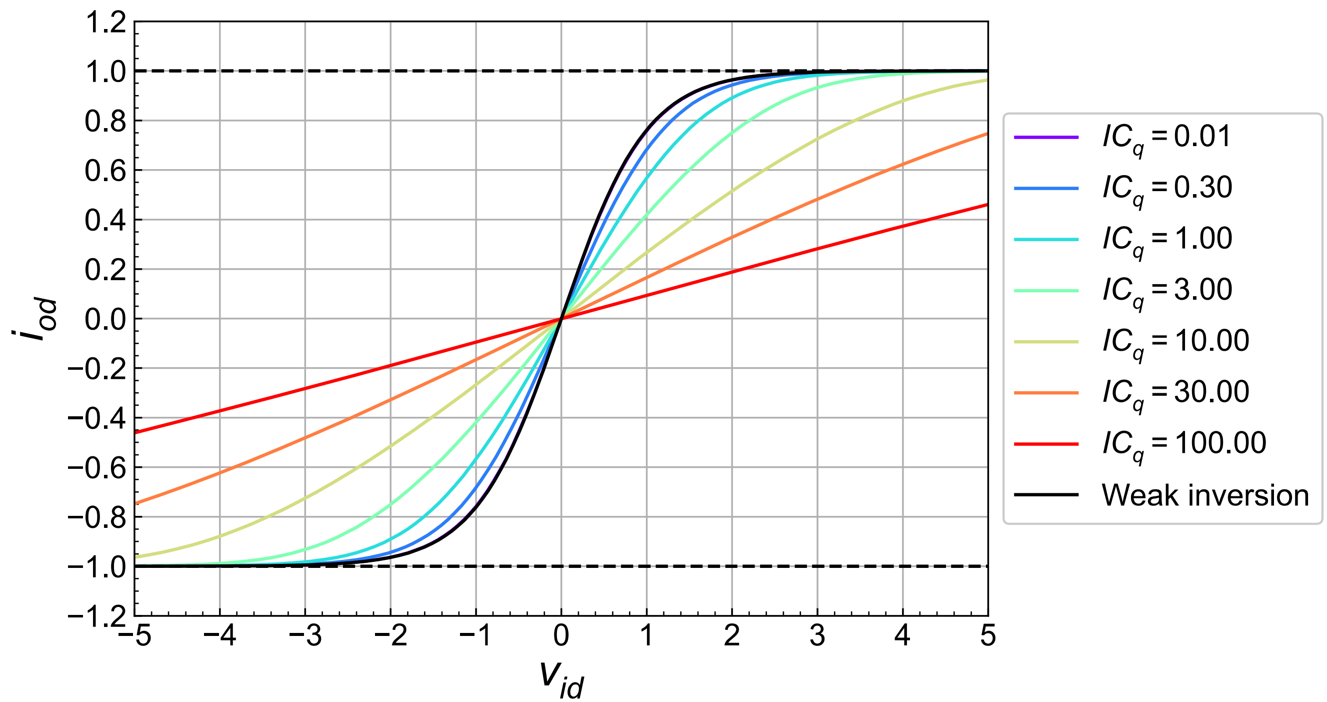



$$I_{od} \triangleq I_1 - I_2$$

$$2I_b = I_1 + I_2$$

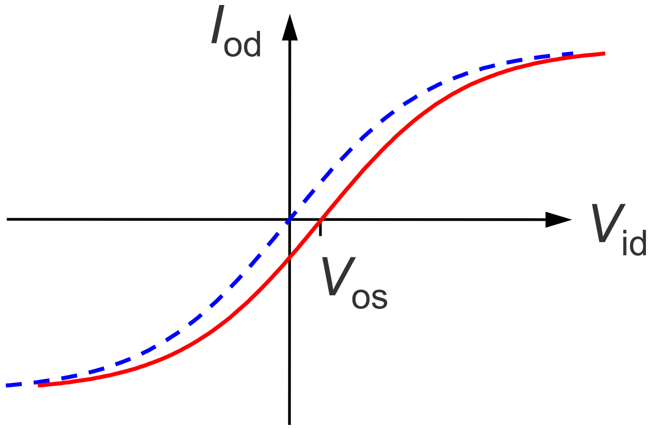
$$V_{id} \triangleq V_{i1} - V_{i2}$$

$$V_{ic} \triangleq \frac{V_{i1} + V_{i2}}{2}$$




- The normalized differential current $i_{od} \triangleq I_{od}/(2I_b)$ can be calculated versus the differential input voltage $v_{id} \triangleq V_{id}/(2nU_T)$ in all regions of inversion defined by the quiescent inversion coefficient $IC_q = I_b/I_{spec}$
- The above plot illustrates how moving to strong inversion extends the linear range

# Effects of Asymmetries – Input Offset Voltage

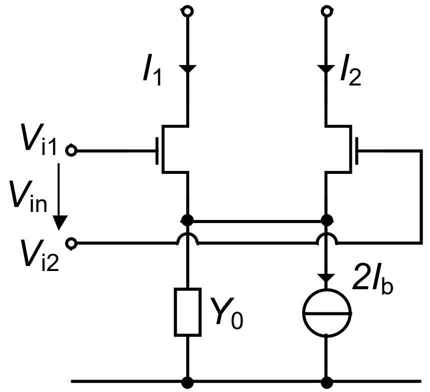



- The mismatch between the two transistors leads to a difference in the output currents $I_1$ and $I_2$ ($I_{od} \neq 0$). This current mismatch can be compensated by a differential input voltage which is defined as the **input-referred offset voltage $V_{os}$**
- Such mismatch can be **deterministic** and caused by either a structural asymmetry due to $\Delta\beta/\beta$ or $\Delta n/n$ or a functional asymmetry due $\Delta I_D/I_D$ (diff. currents imposed in $M_1$ and $M_2$)
- On top of the deterministic mismatch there is also a **random** mismatch due to parameter fluctuation
- The standard deviation of the offset voltage due to random mismatch is given by

$$\sigma_{V_{os}} = \sqrt{\sigma^2_{\Delta V_{T0}} + \left(\frac{I_b}{G_m}\right)^2 \sigma^2_{\frac{\Delta\beta}{\beta}}} = \frac{1}{\sqrt{WL}} \sqrt{A^2_{\Delta V_{T0}} + \left(\frac{I_b}{G_m}\right)^2 A^2_{\beta}}$$

- which is **minimum in weak inversion**

# Effects of Asymmetries – CM Input Voltage to DM Output Current




- One of the most interesting property of the differential pair is its ability to reject any input common-mode (CM) voltage $V_{ic} = (V_{i1} + V_{i2})/2$
- Ideally it fully rejects the CM signal, but due to mismatches and a non-zero admittance $Y_0$ at the common source node, part of the input CM is transformed into a differential output current

# Effects of Asymmetries – Common Mode Rejection Ratio

- Assuming $Y_0 \ll G_m$ (at least correct at DC where $Y_0 = G_{ds}$), the CM transadmittance is given by

$$Y_{cm} \triangleq \frac{I_{od}}{V_{ic}} \cong \frac{Y_0}{2n} \cdot \varepsilon_{g_m} \text{ where } \varepsilon_{g_m} \triangleq \frac{G_{m1} - G_{m2}}{G_m} = \frac{\Delta G_m}{G_m}$$

- The Common Mode Rejection Ratio $CMRR$ is given by

$$CMRR \triangleq \frac{\text{differential gain}}{\text{common mode gain}} = \frac{G_m}{Y_{cm}} \cong \frac{2nG_m}{Y_0 \varepsilon_{g_m}}$$

- Remembering that $G_m = I_D/(nU_T)$ in WI and $G_m = \sqrt{2\beta I_D/n}$ in SI, we get

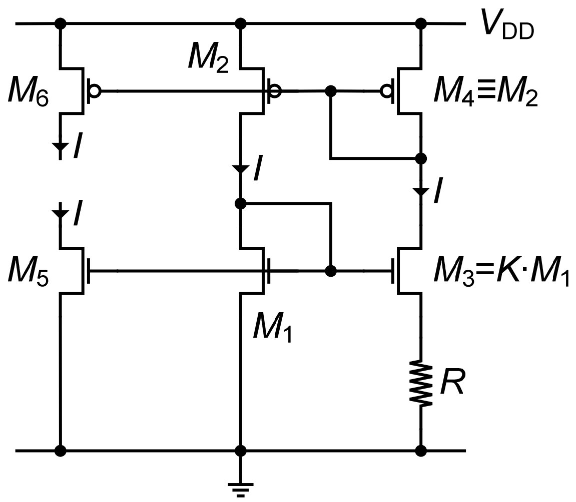
$$\varepsilon_{g_m} \triangleq \frac{G_{m1} - G_{m2}}{G_m} = \frac{\Delta G_m}{G_m} = \begin{cases} \dfrac{\Delta I_D}{I_D} - \dfrac{\Delta n}{n} & \text{WI} \\ \frac{1}{2}\left(\frac{\Delta I_D}{I_D} + \frac{\Delta \beta}{\beta} - \frac{\Delta n}{n}\right) & \text{SI} \end{cases}$$

- The causes of $G_m$ mismatch are
  - structural ($\Delta\beta/\beta$, $\Delta n/n$) or
  - functional ($\Delta I_D/I_D$)

# Outline

- Introduction
- Elementary gain cells (common-source stages)
- Source follower (common-drain stages)
- Cascode stage (common-gate stages)
- Current mirrors
- Differential pair
- **Current references**

# Current Generation – The Vittoz Current Reference




- No "built-in" current available in silicon
  - No way to generate a current that is independent of process parameters
  - Should be independent of the supply voltage

# Current Generation – The Vittoz Current Reference

- $M_1$ and $M_3$ in **weak inversion**:

$$I = \frac{U_T \cdot \ln K}{R}$$

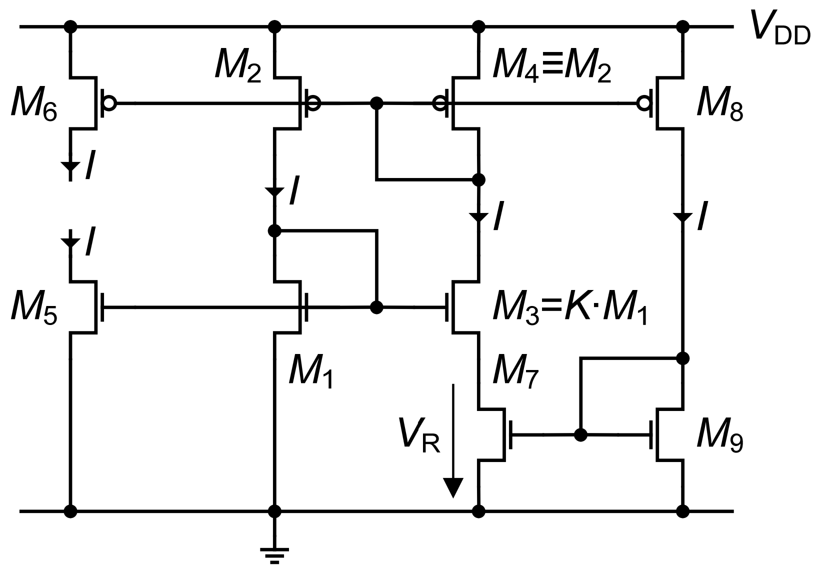
- $n$ times larger if source of M3 connected to (separate) substrate
- **Proportional to absolute temperature** (PTAT) through $U_T$
- Process dependent through $R$
- Should be used to bias transistors operating in weak inversion

- $M_1$ and $M_3$ in **strong inversion**:

$$I = \frac{2\left(\sqrt{K} - 1\right)^2}{n\, R^2\, \beta_3}$$

- $n^2$ times larger if source of M3 connected to (separate) substrate
- **Process (and temperature) dependent** through $R^2 \cdot \beta_3$ term
- Should be used to bias transistors operating in strong inversion

# Current Generation – The Oguey Current Reference




- Resistor can be replaced by transistor $M_7$ in the linear region ($V_R \ll V_{P7}$)
- $M_2 \equiv M_4 \equiv M_6 \equiv M_8$ and $M_1 \equiv M_5$
- $M_7$ and $M_9$ in **strong inversion** with $\beta_7 = A \cdot \beta_9$ ($A \gg 1$ to have $M_7$ in the linear region)
- $M_1$ and $M_3$ in **weak inversion** with $\beta_3 = K \cdot \beta_1$

H. J. Oguey and D. Aebischer, "CMOS Current Reference without Resistance," JSSC, vol. 32, No. 7, July 1997.
C. C. Enz and E. A. Vittoz in *Emerging technologies: Designing Low Power Digital Systems*, R. Cavin and W. Liu, Eds. IEEE, 1996.
P. Heim, S. R. Schultz, and M. A. Jabri, Proc. Sixth Australian Conf. on Neural Networks, Sydney, Australia, 1995, pp. 9-12.

# Current Generation – The Oguey Current Reference

- $V_R$ remains a PTAT voltage given by $V_R = U_T \cdot \ln K$ where $K \triangleq \beta_2/\beta_1$
- The reference current $I_b$ is proportional to $I_{spec7}$

$$I_b = I_{spec7} \cdot \left(\frac{A \ln K}{2}\right)^2 \left(1 + \sqrt{1 + \frac{1}{A}}\right)^2$$

- Which for $A \gg 1$ simplifies to

$$I_b \cong I_{spec7} \cdot (A \ln K)^2$$

- Since $I_{spec6} = A \cdot I_{spec7}$, $I_b$ is also proportional to $I_{spec6}$

$$I_b \cong I_{spec6} \cdot A \cdot (\ln K)^2 \text{ for } A \gg 1$$

- Reference current $I_b$ independent of temperature if mobility $\mu \propto T^{-\alpha}$ with $\alpha \cong 2$
- Useful to bias at inversion coefficient $IC$ independently of the process


📖 H. J. Oguey and D. Aebischer, "CMOS Current Reference without Resistance," JSSC, vol. 32, No. 7, July 1997.

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